1. A structure for split-gate flash memory cells comprising:

a semiconductor region within a substrate;

parallel active regions within said semiconductor region separated by isolation regions;

equally spaced floating gates, composed of a first conductive layer, having sharp corners facing said semiconductor region, which are disposed over said active regions and separated from the active regions by a first insulator layer;

three tiered parallel strips perpendicular to said active regions and passing over said trapezoidal floating gates, comprising a bottom tier covering the trapezoidal floating gates composed of a second insulator layer, a middle tier composed of a second conductor layer and a top tier composed of a third insulator layer;

insulator spacers, composed of a fourth insulator layer, disposed over the sidewalls of said three tiered parallel strips and over the sidewalls of said trapezoidal floating gates, with the parallel structures comprised of said floating gates, said three tiered parallel strips and said insulator spacers being designated floating gate towers;

source/drain regions formed in said semiconductor region below source/drain openings, where source/drain opening is the designation of every other opening between said floating gate towers;

source/drain contact lines composed of a third conductor layer, disposed over said source/drain regions, partially filling said source/drain openings and an insulator layer, composed of a fifth insulator layer, that is disposed over said source drain contact lines;

select gates, composed of said third conductor layer and disposed over a sixth insulator layer that is disposed on said semiconductor region, which are columns rising over said active regions in those openings between said floating gate towers that are not source/drain openings and where the top of said select gates is below the top of said floating gate towers;

parallel select gate contact lines composed of a fourth conductor layer and disposed over said active regions and contacting said select gates.

2. The structure of Claim 1 wherein said semiconductor region is a silicon region.

3. The structure of Claim 1 wherein said isolation regions are shallow trench isolation regions is a silicon region.

4. The structure of Claim 1 wherein said first insulator layer is an oxide layer grown to a depth of about 100 Angstroms.

5. The structure of Claim 1 wherein said floating gates have trapezoidal cross-sections with the sharp cornered base disposed over said first insulator layer.

6. The structure of Claim 1 wherein said second insulator layer is an ONO layer with the top oxide, nitride and bottom oxide component layers each about 60 Angstroms.

7. The structure of Claim 1 wherein said third insulator layer is a nitride layer about 1500 Angstroms thick.

8. The structure of Claim 1 wherein said fourth insulator layer is a high temperature oxide layer about 600 Angstroms thick.

9. The structure of Claim 1 wherein said fifth insulator layer is an oxide layer grown to a depth of about 300 Angstroms.

10. The structure of Claim 1 wherein said sixth insulator layer is an oxide layer grown to a depth of about 150 Angstroms.

11. The structure of Claim 1 wherein said first conductor layer is a polysilicon layer formed to a depth of about 800 Angstroms.

12. The structure of Claim 1 wherein said second conductor layer is a polysilicon layer formed to a depth of about 1000 Angstroms.

13. The structure of Claim 1 wherein said third conductor layer is a polysilicon layer formed to a depth of about 3000 Angstroms.

14. The structure of Claim 1 wherein said fourth conductor layer is a polysilicon layer formed to a depth of about 1500 Angstroms.

15. A method of fabricating split-gate flash memory cells comprising:

providing a semiconductor region within a substrate;

forming isolation regions within said semiconductor region thus defining parallel active regions that are separated by said isolation regions;

forming a first insulator layer over said active regions;

forming a first conductor layer and patterning it into parallel strips disposed over said active regions;

forming three tiered parallel strips running perpendicular to said active regions and passing over said first conductor layer parallel strips, said three tiered parallel strips being comprised of a bottom tier composed of a second insulator layer, a middle tier composed of a second conductor layer and a top tier composed of a third insulator layer;

fashioning said first conductor layer into floating gates having sharp corners facing said semiconductor region;

forming insulator spacers, composed of a fourth insulator layer, disposed over the sidewalls of said three tiered parallel strips and over the sidewalls of said trapezoidal floating gates, the resulting structures comprised of said floating gates, said three tiered

parallel strips and said insulator spacers being designated floating gate towers;

forming source/drain regions in said semiconductor region below source/drain openings, where said source/drain opening is the designation of every other opening between said floating gate towers;

forming source/drain contact lines composed of a third conductor layer and filling said source/drain openings except for a fifth insulator layer that is formed over said source/drain contact lines;

forming select gates, composed of said third conductor layer and disposed over a sixth insulator layer, the sixth insulator layer being formed on said semiconductor region in those openings between floating gate towers that are not source/drain openings, and the select gates being columns rising over active regions in openings between floating gate towers that are not source/drain openings so that the top of said select gates is below the top of said floating gate towers;

forming parallel select gate contact lines composed of a fourth conductor layer and disposed over said active regions and contacting said select gates.

16. The method of Claim 15 wherein said semiconductor region is a silicon region.

17. The method of Claim 15 wherein said isolation regions are shallow trench isolation regions region is a silicon region.

18. The method of Claim 15 wherein said first insulator layer is an oxide layer grown to a depth of about 100 Angstroms.

19. The method of Claim 15 wherein said floating gates have trapezoidal cross-sections with the sharp cornered base disposed over said first insulator layer.

20. The method of Claim 15 wherein said second insulator layer is an ONO layer with the top oxide, nitride and bottom oxide component layers are each about 60 Angstroms, respectively.

21. The method of Claim 15 wherein said third insulator layer is a nitride layer about 1500 Angstroms thick.

22. The method of Claim 15 wherein said fourth insulator layer is a high temperature oxide layer about 600 Angstroms thick.

23. The method of Claim 15 wherein said fifth insulator layer is an oxide layer grown to a depth of about 300 Angstroms.

24. The method of Claim 15 wherein said sixth insulator layer is an oxide layer grown to a depth of about 150 Angstroms.

25. The method of Claim 15 wherein said first conductor layer is a polysilicon layer formed to a depth of about 800 Angstroms.

26. The method of Claim 15 wherein said second conductor layer is a polysilicon layer formed to a depth of about 1000 Angstroms.

27. The method of Claim 15 wherein said third conductor layer is a polysilicon layer formed to a depth of about 3000 Angstroms.

28. The method of Claim 15 wherein said fourth conductor layer is a polysilicon layer formed to a depth of about 1500 Angstroms.